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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/671,889	09/29/2003	Fred Gehrung Gustavson	YOR920030170US1	8009

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EXAMINER	
VICARY, KEITH E	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/671,889	GUSTAVSON ET AL.	
	Examiner	Art Unit	
	Keith Vicary	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :9/11/2006, 11/21/2006, 2/27/2007.

DETAILED ACTION

1. Claims 1-19 are pending in this application and presented for examination.

Specification

2. The disclosure is objected to because of the following informalities. Appropriate correction is required.

a. The application numbers of the co-pending applications listed on pages 1 and 2 of the specification should be filled in where blank.

b. "exempalry," on page 4, line 7, should be "exemplary."

Double Patenting

3. Claims 1-19 of this application conflict with claims 1, 3-6, 8-12, and 14-19 of Application No. 10671937. 37 CFR 1.78(b) provides that when two or more applications filed by the same applicant contain conflicting claims, elimination of such claims from all but one application may be required in the absence of good and sufficient reason for their retention during pendency in more than one application. Applicant is required to either cancel the conflicting claims from all but one application or maintain a clear line of demarcation between the applications. See MPEP § 822.

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct

from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-19 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3-6, 8-12, and 14-19 of copending Application No. 10671937. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-19 of the instant application are obvious variants of claims 1, 3-6, 8-12, and 14-19 of the '937 application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

6. Claims 1-19 of the instant application contain every limitation of claims 1, 3-6, 8-12, and 14-19 of the '937 application; moreover, claims 1-19 of the instant application claim prefetching data into a cache providing data into an FPU, whereas claims 1, 3-6, 8-12, and 14-19 of the '937 application merely claim preloading data into a floating point register of an FPU.

It would have been readily recognized by one of ordinary skill in the art at the time of the invention that the benefits of using cache in the instant application are numerous and include greater system performance due to the decreased access time to access cache in comparison to main memory combined with the locality of reference that is typical in most computer programs.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement cache into the instant application to gain greater system performance; it would have been readily recognized by one of ordinary skill in the art at the time of the invention that greater system performance is desirable in any processor. Furthermore, it would have been readily recognized by one of ordinary skill in the art at the time of the invention that this cache would fit into the '937 application by receiving data from the main memory and sending it to the floating point register, and that when preloading data into the floating point register in a system which uses a cache, that data would have to be prefetched into the cache in order to be preloaded into the register.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the widely-known teachings of cache with the invention of the '937 application in order to increase system performance.

c. Further note that claims 2, 11, and 13 in the instant application also claim that prefetching data is accomplished by utilizing time slots caused by a difference between a time to execute instructions in said subroutine execution

process and a time to load said data, while claims 1, 11, and 12 of the '937 application does not explicitly disclose this.

It would have been readily recognized by one of ordinary skill in the art at the time of the invention that prefetching data in general cuts down the amount of time a processor is waiting for a memory miss to be serviced, and prefetching by utilizing time slots caused by a difference between a time to execute instructions and a time to load said data allows for data to be prefetched ahead of time without delaying any other instructions that are being processed. Furthermore, it would have been readily recognized by one of ordinary skill in the art at the time of the invention that the benefits of prefetching are contingent upon other instructions not being delayed due to the prefetching; thus, it would have been readily recognized to one of ordinary skill in the art at the time of the invention that prefetching would be done by utilizing these time slots of inactivity.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the widely-known method of prefetching by utilizing time slots with the '937 application in order to cut down the amount of time a processor is waiting for a memory miss to be serviced, thus increasing overall system performance.

7. Aside from the obvious variants listed above, claim 1 of the '937 application contains every element of claim 1 of the instant application.

8. Aside from the obvious variants listed above, claim 1 of the '937 application contains every element of claim 2 of the instant application.

9. Aside from the obvious variants listed above, claim 3 of the '937 application contains every element of claim 3 of the instant application.

10. Aside from the obvious variants listed above, claim 4 of the '937 application contains every element of claim 4 of the instant application.

11. Aside from the obvious variants listed above, claim 5 of the '937 application contains every element of claim 5 of the instant application.

12. Aside from the obvious variants listed above, claim 6 of the '937 application contains every element of claim 6 of the instant application.

13. Aside from the obvious variants listed above, claim 8 of the '937 application contains every element of claim 7 of the instant application.

14. Aside from the obvious variants listed above, claim 9 of the '937 application contains every element of claim 8 of the instant application.

15. Aside from the obvious variants listed above, claim 10 of the '937 application contains every element of claim 9 of the instant application.

16. Aside from the obvious variants listed above, claim 11 of the '937 application contains every element of claim 10 of the instant application.

17. Aside from the obvious variants listed above, claim 6 of the '937 application contains every element of claim 11 of the instant application.

18. Aside from the obvious variants listed above, claim 12 of the '937 application contains every element of claim 12 of the instant application.

19. Aside from the obvious variants listed above, claim 12 of the '937 application contains every element of claim 13 of the instant application.

20. Aside from the obvious variants listed above, claim 14 of the '937 application contains every element of claim 14 of the instant application.

21. Aside from the obvious variants listed above, claim 15 of the '937 application contains every element of claim 15 of the instant application.

22. Aside from the obvious variants listed above, claim 16 of the '937 application contains every element of claim 16 of the instant application.

23. Aside from the obvious variants listed above, claim 17 of the '937 application contains every element of claim 17 of the instant application.

24. Aside from the obvious variants listed above, claim 18 of the '937 application contains every element of claim 18 of the instant application.

25. Aside from the obvious variants listed above, claim 19 of the '937 application contains every element of claim 19 of the instant application.

Claim Rejections - 35 USC § 112

26. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

27. Claims 1-5 and 11-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

28. In claims 1, 12, and 17, it is indefinite as to what "unrolling instructions" is. For the purposes of this office action, the examiner is interpreting the limitation as "unrolling loops into instructions." Furthermore, it is indefinite as to what "unrolling causing said instructions to touch data" is. Under the examiner's previous interpretation of "unrolling instructions" as "unrolling loops into instructions," it is unclear how the unrolling of loops into instructions would cause those instructions to touch data, and it is unclear as to how touch instructions could result from the unrolling of loops.

d. Claims 2-5, 13-16, and 18-19 are rejected for failing to alleviate the rejections of claims 1, 12, and 17 above.

29. In claims 2, 11, and 13, it is indefinite as to what "utilizing time slots" entails. Furthermore, it is indefinite as to what "a time to execute instructions in said subroutine execution process" is, as it is always time to execute instructions during an execution process. It is also indefinite as to what constitutes a "time slot," and how they are "caused" as opposed to just existing.

30. Claims 2, 11, and 13 recite the limitation "said subroutine execution process" in line 3. There is insufficient antecedent basis for this limitation in the claim.

31. Claims 3, 4, 14, and 15 recite the limitation "matrix subroutine" in line 1. There is insufficient antecedent basis for this limitation in the claim.

e. Claim 5 is rejected for failing to alleviate the rejection of claim 4 above.

32. Claim 16 recites the limitation "said LAPACK subroutine" in line 1. There is insufficient antecedent basis for this limitation in the claim. For the purposes of this office action, the examiner is reading "the signal-bearing medium of claim 12" in line 1 of claim 16 to read "the signal-bearing medium of claim 15," due to the dependency on claim 5 on claim 4, the dependency of claim 9 on claim 8, and the dependency of claim 19 on claim 18, all of which claim the same limitations as claims 15 and 16.

Claim Rejections - 35 USC § 101

33. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

34. Claims 1-5 and 12-19 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

f. A claim to an abstract idea must effect a useful, concrete, and tangible result. The tangible requirement requires that the claim must set forth a practical application of that abstract idea to produce a real-world result, and not just something that has been determined that has not been made available for use through some form of conveyance or at least temporary storage somewhere.

g. In an apparatus claim, if programmed functionality is being relied upon for patentability as opposed to the arrangement of hardware, said programmed functionality must effect a useful, concrete, and tangible result.

35. In claims 1, 12, and 17, the limitation "unrolling instructions" does not set forth a practical application to produce a real world result, as unrolling instructions is merely a preliminary step in the practical application of executing a linear algebra routine. Note that the limitations "to prefetch data" and "to touch data" as written constitute intended use and does not necessarily cause any functionality or recited act to occur. Further note that even if these limitations were written in a manner that is not intended use, claim 6 discloses that memory is touched *to be loaded* into said cache, which implies that the touching of memory does not cover the actual prefetching of data into a cache, but rather only the preliminary step of determining which data will be prefetched into the cache in the future, which would make the touching of memory an intangible result as well.

h. Claims 2-5, 13-16, and 18-19 are rejected for failing to alleviate the rejection of claims 1, 12, and 17 above.

36. Claim 12 is not limited to tangible embodiments. In view of Applicant's disclosure, specification page 20, lines 9-15, the signal-bearing medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., DASD storage, magnetic tape, electronic read-only memory, an optical storage device, paper "punch cards") and intangible embodiments (e.g., other suitable signal-bearing media including transmission media such as digital and analog and communication links and wireless). As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

i. Claims 13-16 are rejected for failing to alleviate the rejection of claim 12 above.

37. To alleviate this rejection, the examiner recommends amending the specification to clearly label the aforementioned tangible embodiments as types of storage medium and the aforementioned intangible embodiments as types of transmission medium, and then subsequently amend the claim to disclose the storage medium instead of the signal-bearing medium.

Claim Rejections - 35 USC § 102

38. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

39. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Gustavson et al. (Gustavson) (Superscalar GEMM-based Level 3 BLAS – The On-going Evolution of a Portable and High-Performance Library, Para'98, pages 207-215).

40. Consider claim 1, Gustavson discloses a method of executing a linear algebra subroutine, said method comprising: for an execution code (section 1, line 6, BLAS code) controlling an operation of a floating point unit (FPU) (section 3.1, line 4, discloses floating point registers, therefore it is inherent there are floating point units that are doing the multiplications as in section 1, line 2) performing a linear algebra subroutine execution (section 1, line 8, routine along with section 1, line 1, linear algebra), unrolling

instructions (section 3.1, line 1, loop unrolling) to prefetch data (section 4.1, line 4, prefetching) into a cache (section 4.1, line 4, cache) providing data into said FPU (section 4.1, line 1, data, and section 4.1, line 10, BLAS, which uses the FPUs), said unrolling causing said instructions to touch data anticipated for said linear algebra subroutine execution (section 4.1, line 12, touch).

41. Consider claim 6, Gustavson discloses an apparatus, comprising: a memory to store matrix data to be used for processing in a linear algebra program (section 4, line 12, shared main memory and section 4.2, lines 7-9, elements of the matrix); a floating point unit (FPU) to perform said processing (section 3.1, line 4, discloses floating point registers, therefore it is inherent there are floating point units that are doing the multiplications as in section 1, line 2); a load/store unit (LSU) to load data to be processed by said FPU (section 3.1, lines 6-7, load and store operations, thus it is inherent there is a load/store unit), said LSU loading said data into a plurality of floating point registers (FRegs) (section 3.1, line 4, floating point registers); and a cache to store data from said memory and provide said data to said Fregs (section 4.1, line 4, cache), wherein said matrix data in said memory is touched to be loaded into said cache prior to a need for said data to be in said FRegs for said processing, (section 4.1, line 12, touch instruction).

42. Consider claim 12, Gustavson discloses a signal-bearing medium tangibly embodying a program of machine-readable instructions executable by a digital

processing apparatus to perform a method of executing linear algebra subroutines, said method comprising: for an execution code (section 1, line 6, BLAS code) controlling an operation of a floating point unit (FPU) (section 3.1, line 4, discloses floating point registers, therefore it is inherent there are floating point units that are doing the multiplications as in section 1, line 2) performing a linear algebra subroutine execution (section 1, line 8, routine along with section 1, line 1, linear algebra), unrolling instructions (section 3.1, line 1, loop unrolling) to prefetch data (section 4.1, line 4, prefetching) into a cache (section 4.1, line 4, cache) providing data into said FPU (section 4.1, line 1, data, and section 4.1, line 10, BLAS, which uses the FPUs), said unrolling causing said instructions to touch data anticipated for said linear algebra subroutine execution (section 4.1, line 12, touch).

43. Consider claim 17, Gustavson discloses a method of providing a service involving at least one of solving and applying a scientific/engineering problem, said method comprising at least one of:

using a linear algebra software package that computes one or more matrix subroutines, wherein said linear algebra software package generates an execution code (section 1, line 6, BLAS code) controlling an operation of a floating point unit (FPU) (section 3.1, line 4, discloses floating point registers, therefore it is inherent there are floating point units that are doing the multiplications as in section 1, line 2) performing a linear algebra subroutine execution (section 1, line 8, routine along with section 1, line 1, linear algebra), unrolling instructions (section 3.1, line 1, loop unrolling) to prefetch

data (section 4.1, line 4, prefetching) into a cache (section 4.1, line 4, cache) providing data into said FPU (section 4.1, line 1, data, and section 4.1, line 10, BLAS, which uses the FPUs), said unrolling causing said instructions to touch data anticipated for said linear algebra subroutine execution (section 4.1, line 12, touch); providing a consultation for solving a scientific/engineering problem using said linear algebra software package (it is inherent that the BLAS will solve some type of scientific/engineering problem for someone who may or may not be the operator of the BLAS program); transmitting a result of said linear algebra software package on at least one of a network, a signal-bearing medium containing machine-readable data representing said result, and a printed version representing said result; and receiving a result of said linear algebra software package on at least one of a network, a signal-bearing medium containing machine-readable data representing said result, and a printed version representing said result (it is inherent that the result of the problem will be conveyed to someone who may or may not be the operator of the BLAS program; furthermore, it is inherent that the result can only be shown either through a printout or through some type of electronic means, which encompasses voice through a phone or data through a network that is read via a monitor).

44. Consider claims 2, 11, and 13, Gustavson discloses said prefetching data is accomplished by utilizing time slots caused by a difference between a time to execute instructions in said subroutine execution process and a time to load said data. As explained above, it is inherent to prefetching that data is loaded into the cache before

the instruction that needs that data is executed, thus there must be a difference between the time of that instruction execution and the time of its data loading, otherwise it would not be prefetching. Furthermore, Gustavson discloses in page 12, lines 2-3 of section 4.1 that the prefetching instruction does not disturb ongoing computations and data references, thus this prefetching must be done in "time slots" which are independent of other instruction fetching.

45. Consider claims 3, 7, and 14, Gustavson discloses said matrix subroutine comprises a matrix multiplication operation (section 1, line 2, matrix multiply).

46. Consider claims 4, 8, 15, and 18, Gustavson discloses said matrix subroutine comprises a subroutine from a LAPACK (Linear Algebra PACKage) (section 1, line 1, discloses a BLAS, which is a part of LAPACK).

47. Consider claims 5, 9, 16, and 19, Gustavson discloses said LAPACK subroutine comprises a BLAS Level 3 L1 cache kernel (Abstract, lines 1-6, level 3 BLAS kernel and level 1 cache).

48. Consider claim 10, Gustavson discloses a compiler to generate instructions for said touching (section 4.1, lines 2-4, compiler)

Conclusion

49. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571) 270-1314. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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